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Challenges and Innovations in Multi-Patterning Lithography for Advanced Node Technologies: Addressing Line Edge Roughness and Critical Dimension Variability

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As semiconductor manufacturing advances to smaller technology nodes, Multi-Patterning Lithography (MPL) has become essential for extending the capabilities of optical lithography. However, MPL introduces significant challenges, including Line Edge Roughness (LER) and Critical Dimension (CD) variability, which can impact device performance and yield. This study explores the technical hurdles associated with MPL and examines emerging innovations to mitigate these effects. Advanced process control strategies, including computational lithography, machine learning-driven metrology, and novel resist materials, are evaluated for their effectiveness in improving pattern fidelity. Additionally, the role of self-aligned patterning techniques, etch process optimizations, and next-generation lithographic solutions, such as Extreme Ultraviolet (EUV) and high-NA lithography, is analyzed. This research provides insights into the evolving landscape of semiconductor fabrication, emphasizing the balance between cost, complexity, and precision in achieving high-resolution, high-yield manufacturing for advanced node technologies.