DOI: doi.org/10.47363/JAICC/ICAICC/2025(4)001

International Conference on
Artificial Intelligence and Cloud Computing (ICAICC-2025)

Conference Proceeding May 08, 2025 - Florida, USA

Optimized Asynchronous FPGA Designs for Efficient AI Acceleration

Floren Deeg

FPGA Developer, Germany

This work presents a connection between asynchronous circuits and artificial intelligence (AI), with a particular focus on the implementation and optimization of asynchronous designs in Field-Programmable Gate Array (FPGA) architectures. It is demonstrated how low-level asynchronous circuits can be designed with the specific intention of being used with FPGAs. This allows the inherent advantages of asynchronous systems, such as reduced latency and energy efficiency, to be utilized for AI workloads. FPGAs are employed in this context as accelerating hardware platforms, which represent a promising solution for AI applications due to their flexibility and performance. The results illustrate the potential of asynchronous FPGA designs as efficient accelerators for AI and open up new avenues for the development of energy-efficient, high-performance hardware solutions in artificial intelligence.